This project simulates a simplified CPU with an MMU, OS, memory, and peripherals to model the fetch, decode and execute cycle of the CPU.

1. CPU (Central Processing Unit)

- Fetches instructions from memory.

- Decodes the instruction

- Executes the instruction fetched from memory.

- Communicates with the MMU for memory access.

- Supports basic arithmetic and logical operations.

- Contains registers for temporary data storage.

- Program Counter, which points to the next instruction, in the code section in memory.

- Accumulator, which the logical operations work on.

- Instruction Register, holds the instruction in use.

- Memory Address Register, which holds the address for the memory.

- Memory Data Register, which hold either the instruction or data from memory.

The CPU has a few registers, used to store temporary data used to execute an instruction.

First the Program Counter (PC), which is used to point towards the next instruction in memory. The value stored is the virtual address not the physical address, so it needs to get translated by the MMU. This translated physical address is then stored in the Memory Address Register (MAR). During the fetching stage, the CPU looks at the Program counter, then asks the MMU to translate this virtual address to a physical one. The resulting physical address is then stored at the MAR. After this steps the CPU retrieves the instruction stored at the address inside the MAR. This retrieved instruction is temporary stored at the Memory Data Register (MDR). This register holds the retrieved data from memory, as such it doesn’t need to hold an instruction. If it is an instruction however, the next step is to store this to a register called Instruction register (IR), which holds the current running instruction, used for the other stages. After this is done, the program counter is increased by two, as as instruction uses two memory locations. One for the opcode/optype and the other is for the operand. These three values gets put into a instruction struct, and this struct is what is stored inside the IR. THis ends the fetching stage, and we proceed to the decoding stage.

At the decoding stage the CPU interprets the instruction. In my implementation it looks at the optype. This optype is a true or false indicating whether it needs to access the memory. If the optype is 0 (false), it interprets the operand as an actual value to be used at a later step. This value gets stored in the MDR, and the step is done. If the optype is 1, it skips this step. The optype being 1, indicates that the operand is a virtual address to be used to access memory, and the value stored at this memory location is what is stored inside the MDR to be used for the later operation, e.g ADD. However this memory accessing is also done in the execution stage, so the decoding stage is only to decipher the optype.

The next and last stage is the execution stage, where the instruction is executed. First it checks if it needs to access the memory, from the decoding stage. If it does, it does so first. Then the CPU proceeds to execute the opcode stored in the IR. These opcodes are mapped to operation functions stored inside the CPU. So it looks for the corresponding function for the opcode, and runs the function. This concludes the fetch-decode-execute cycle.

There are however one register not touched upon, which is used for the specific operation, namely the Accumulator (AC). It is this value that gets worked on by the operations. Lets look at the ADD operation. As the name suggests it adds a value on top of another, and the other being the accumulator. So it takes the current value in the accumulator, and adds the new value from the MDR. You can’t specify which value to add to, everything goes through the accumulator.

The same applies to the STORE operation, which stores the current value in the accumulator and stores it into a memory address.

Operations:

ADD:

Adds the specified value to the accumulator.

OldAccumulator + Value = NewAccumulator

SUB:

Subtract the specified value from the accumulator.

OldAccumulator - Value = NewAccumulator

STORE :

Stores the current value in the accumulator, to the specified memory address.

LOAD

Retrieves the value from the specified memory address, and sets the accumulator to it.

JUMP:

Sets the Program Counter to the specified value.

Note: The specified value can be directly from the operand, or from a stored memory address. Remember Optype.

2. MMU (Memory Management Unit)

- Translates virtual addresses to physical addresses.

- Reads from memory.

- Writes to memory.

1. OS (Operating System)

- The entity of that govern the other entities, like cpu, memory, scheduler, process controller.

- Initialize the required components:

- CPU

- Memory

- ProcessTable

- CPU Controller

- Scheduler

- FreeList

- Start/Stop/Pause/Resumes the simulation.

- Schedules processes.

1. Memory (RAM)

- Stores code, stack and heap, of various processes.

- Accessible by the CPU via the MMU.

5. Scheduler

- Manages the process queue, for which to run.

6. Process Controller

- Create a new process.

- Control the allocation of memory space.

- Store instructions

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MMU functions:

func (mmu \*MMU) TranslateAddress(virtualAddr uint32) (int, error) {}

Takes in a virtual address, and returns the physical address given after a translation. This physical address is used to access the physical memory.

func (mmu \*MMU) Read(physicalAddr uint32) (int, error) {}

Takes in a physical address, reads from memory at that address, and returns the stored value at this address.

func (mmu \*MMU) Write(physicalAddr uint32, value uint32) error {}

Takes in a physical address and a uint32 value, goes to that memory address, and replaces the currently stored value, with the new one.